IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Jeffrey S. Mailloux et al.	Examiner: Hong Kim
Serial No.:	08/650,719	Group Art Unit: 2185
Filed:	May 20, 1996	Docket: 303.623US1
Title:	ASYNCHRONOUSLY-ACCESSIBLE MEMORY DEVICE WITH MODE SELECTION CIRCUITRY FOR BURST OR PIPELINED OPERATION	

REPLY BRIEF UNDER 37 CFR § 41.41

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This Reply Brief is presented in response to the Examiner's Answer, dated October 31, 2007, which was sent as a reply to Appellants' Appeal Brief, filed on August 13, 2007. Appellants' Appeal Brief was filed in response to the rejection of claims 1-9, 33-35, 46, 48-50, 59-61 and 63-64 in the above-identified Application, as set forth in the Final Office Action dated February 20, 2007 ("Final Office Action"). Please charge any required additional fees or credit overpayments to Deposit Account 19-0743.

REMARKS

The Examiner's Answer Brief, ("Examiner's Answer") dated October 31, 2007, includes substantially identical grounds for rejection as the Final Office Action. Appellants respectfully maintain that the arguments presented in the Appeal Brief, which is hereby incorporated by reference and reasserted in response, remain compelling and overcome the original grounds of rejection.

Status of the Claims

The present Application was filed on May 20, 1996 with claims 1-58. Claims 11-32, 36-45, and 51-58 were canceled in response to a restriction requirement, the response being filed on November 3, 1997. Claims 10 and 47 were canceled, and claims 3-9, 33-35, 46, and 48-50 were amended in a response filed on December 7, 1998. Claims 1, 33, and 50 were amended in a response filed on April 27, 1999. Claim 50 was amended in a response filed on September 2, 1999. At this point, claims 1-9, 33-35, 46, and 48-50 were pending.

Claim 50 was amended, and new claims 59-64 were added in a response filed on September 30, 1999. Claims 46 and 61 were amended in a response filed on March 19, 2000. Claim 62 was canceled in response to a restriction requirement, the response being filed on November 7, 2000. Claim 61 was amended in a response filed on May 2, 2001. Claim 7 was amended in a response filed on May 31, 2002, and again in a response filed on September 16, 2002. Finally, claim 61 was amended in a response filed December 22, 2006. Claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 stand twice rejected and are the subject of the present Appeal.

Response by the Appellants to the Arguments in the Answer

While the Appellants believe the arguments presented in the Appeal Brief remain compelling and complete, the following set of brief remarks is presented in light of the Examiner's Answer, so as to more precisely focus and highlight the respective positions of the Appellants and the Examiner.

With Respect to Section A.

The Examiner asserts that Manning discloses a memory selectively operable either in a burst mode or fast page mode, EDO page mode, and static column mode. As stated by the Board of Patent Appeals and interferences (BPAI), "Manning provides no details as to how the use of a pipelined structure might be accomplished. We agree with appellants. Manning's suggestion to use a pipeline architecture is insufficient to suggest switching between burst and pipelined modes. As indicated supra, we find nothing in Manning to suggest substituting a pipelined mode for the standard EDO such that selecting or switching between burst and pipelined modes can occur. Accordingly, we cannot sustain the obviousness rejection ...". BPAI, Appeal No. 2005-1725, March. 20, 2006. Thus, Manning fails to teach switching between burst and pipelined modes.

The Examiner states in the Examiner's Answer, "In other words, the pipelined architecture can be used on the fast page mode, EDO page mode, static column mode and burst operation in order to increase accessing speed." It should be noted that a pipelined architecture of Manning does not equal the pipelined mode claimed by Appellants. As noted in the Appeal Brief filed by Appellants in a related matter (Application Ser. No. 08/984,701 and 08/984,563), another way of viewing whether they are the same is to ask the question: how can a memory have a pipelined architecture (as mentioned by Manning) without inherently operating in the pipelined mode claimed by the Appellants? The brief answer is that a memory, such as a burst EDO memory, may include pipelined registers that permit the rapid generation of internal addresses. However, external addresses are still received and processed in the same fashion as regular EDO memory.

Burst EDO memory improves EDO performance by adding a pipeline stage (i.e. a pipelined architecture) to permit reads or writes to occur in four row-address bursts. After the initial page address is applied to a burst EDO chip, the chip typically provides three more sequential addresses (within a page). This address circuitry eliminates the time required to detect and latch externally supplied addresses. However, burst EDO memory including a pipelined architecture *does not accept external addresses so as to operate in a pipelined mode* (as defined by the Appellants in the Application).

A true pipelined mode of operation makes use of time slicing address information so that external accesses to a memory may overlap internal operations without conflicting. This allows for a continuous data stream of address information in the form of external addresses. Thus, *internal addresses are not generated in pipelined mode*. Rather, addresses are provided from an external source as a stream of data.

In addition, Roy does not disclose the "pipeline mode" as recited in the rejected claims. Roy describes a memory device capable of column burst activity where sequential bytes of data are accessed using a starting column and row address and a burst length. *See* Roy, Col. 26, lines 62-66. New actions may be initiated when a burst is completed. *See Id.* at Col. 27, lines 4-14. The device may also be used in a "pseudo-pipelined" access mode, such that a new column address is provided every cycle for a random read operation, as long as it is confined to a selected row. *See Id.* at Col. 28, lines 16-32 and Col. 33, lines 8-19. While limited access pseudo-pipelined reads may occur once per cycle, pseudo-pipelined write operations occur at only one-half the maximum channel frequency, since channel access is shared by both addresses and data. *See Id.* at Col. 33, lines 65-67. This is in direct contrast to the teachings of the Appellants, which enable true pipelined operation, with column-based switching in addition to row-based switching (See Application, pg. 38, lines 7-16).

Ogawa does not teach any kind of switching behavior. Pipelined access in Ogawa is described solely with respect to a single mode of operation – the page mode. *See* Ogawa, Abstract and Col. 1, lines 8-12. "The page mode processing is an operation that subsequently reads out data in memory cells connected to one word line selected by a row address by sequentially changing the column address ...". Col. 4, lines 4-8. While Ogawa notes that "the present invention is not limited to the page mode, and the concept of the present invention can be similarly applied to random read/write operation" at Col. 12, lines 5-10, this statement of potential use with respect to random read/write operations does not lead one of ordinary skill to understand how switching between burst and pipelined modes would be accomplished, since Ogawa does not teach any kind of switching behavior. As such, Ogawa provides no indication of how memory access operations can be conducted in conjunction with switching between burst a pipelined modes "on the fly" as taught by the Appellants.

Therefore, no combination of Manning and either Roy or Ogawa can provide a device "configured to switch between the pipelined mode and the burst mode for operating the asynchronously-accessible storage device in either mode" (claim 1) or "selecting between an asynchronously-accessible burst mode and an asynchronously-accessible pipelined mode of operation of the storage device" (claim 33), much less "providing a new external address for every access associated with asynchronously accessing the asynchronously-accessible memory device while in the pipelined mode of operation; switching modes to a burst mode of operation" (claim 46) as claimed by the Appellants.

With respect to Section B.

The Examiner states that, "It is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously and also It was well known in the memory art to include the memory selectively operable in a pipeline mode in the same field of endeavor for the purpose of increasing the throughput by accessing the memory every cycle. In other words, the pipelined architecture advantage in a memory effectively hides memory wait state, specifically this is accomplished by overlapping memory operations using a pipe." In addition the Examiner states, "The ability to provide a new column address every cycle would have a highly desirable feature in the memory environment of Manning because one of the objectives of memory access is increasing throughput or speed. Also the ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory operable in a pipeline mode." The use of unsupported assertions in the Office Action does not satisfy the explicit requirements needed to demonstrate motivation as set forth by the *In re Sang Su Lee* court. Therefore, the Examiner appears to be using personal knowledge, and is again respectfully requested to submit an affidavit as required by 37 C.F.R. § 1.104(d)(2). To-date, no such affidavit has been provided.

CONCLUSION

Appellants respectfully submit that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone the Appellants' attorney at (210) 308-5677 to facilitate prosecution of this application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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